Semiconductors

AN10006_2

Designing a Hi-Speed USB Host PCI Adapter Using the ISP1561

May 2004

Application Note
Rev. 2.0

Revision History:

Version	***Date***	***Description***	***Author***
2.0	May 2004	Updated the schematics and updated to the latest template.	Kunzang DOLMA
1.3	July 2002	• Revised the file name from "DESIGNING_A_USB20_HOST_PCI_ADAPTER_USING_ISP1561_2. pdf" to AN10006-01.pdf • Contents update.	Socol Constantin, Adrian Albu.
1.2	Feb 2002	Added content to the following sections: • Introduction • Description of the application Schematic • PCB Design Recommendations • Added the section New features in ISP1561 ES3	Socol Constantin
1.1	July 2001	• Revised schematics • Corrected V_{AUXA} and V_{AUXD} to AV_{AUX} and DV_{AUX} • Mention of PolySwitch removed • PCI pin names reverted to PCI spec conventions • Made consistent the example of MIC2026	Socol Constantin, Adrian Albu
1.0	June 2001	First release	Socol Constantin

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1. Introduction

The ISP1561 is a Hi-Speed Universal Serial Bus (USB) Host Controller (HC) that can be directly connected to a standard 32-bit, 33 MHz PCI bus. The ISP1561 is compliant with *PCI Local Bus Specification Revision 2.2* and *PCI Bus Power Management Interface Specification Revision 1.1*. No additional logic is necessary to implement a complete Hi-Speed USB Host Controller solution on PCI.

Adapter cards based on the ISP1561 implement three functions: function 0 and function 1 for OHCI1 and OHCI2, and function 2 for EHCI. According to the PCI Local Bus Specification, each physical PCI device may incorporate one to eight separate functions (logical devices). Each function contains its own memory-mapped individually addressable configuration space (according to the USB specification: 4 kbytes each for OHCI1 and OHCI2, and 256 bytes for EHCI) containing configuration registers.

The configuration registers of the ISP1561 are used by the system's BIOS and the operating system to detect the presence of the respective functions (vendor ID (VID) and product ID (PID)), and determine the necessary resource requirements (memory and I/O space, interrupt lines, and so on) and specific capabilities.

A set of on-chip "operational" registers is also defined for each of the three Host Controllers implemented in the ISP1561. The respective Host Controller device driver interacts with these registers to implement the USB functionality and the legacy support. A detailed description of configuration registers and operational registers can be found in the ISP1561 data sheet.

The ISP1561 implements two internal "power wells"—V_{DD} and V_{DDX}—to benefit from the PCI V_{AUX} = 3.3 V dedicated power source, which is present on the PCI connector (pin A14) even when PCI V_{CC} = 3.3 V is OFF. This enables the ISP1561 PME# signal to be asserted and activates the wake-up logic of the motherboard even if the rest of the system is powered down (for example, in the S3cold system standby mode). This is applicable mainly to on-board (desktop) or mobile designs, but not applicable to PCI add-on cards because the PCI +5 V (used for V_{BUS}) is also OFF during S3cold.

The ISP1561 may use the PCI V_{AUX} to power its four internal transceivers (connected to the ISP1561 AV_{AUX} (analog)), and also the clock circuitry, Port Router, Root Hub and Power Management Event (PME#) logic (connected to the ISP1561 DV_{AUX} (digital)).

For details on implementation of the PCB design, see Section 3.

The power management capabilities enabled by using V_{AUX} allow system designers to meet the governmental energy regulations that are becoming increasingly essential worldwide (Energy Star/USA—30 W standby, White Swan/Europe—5 W standby, Blue Angel/Europe—5 W standby).

This document contains a description of the application schematics and the PCB design recommendations.

2. Description of the Application Schematics

The schematics (see Section 4) contain a complete implementation of the ISP1561 and allow testing of all its features in different types of design: PCI add-on card, on-board design in standard desktop or mobile solution.

In case of a standard PCI add-on card design, some simplifications to the schematics (see Section 4) can be done, as described here. Some features will not be normally used in a standard PCI add-on card, for example, the legacy support, wake-up from S3cold (no external +5 V input for V_{BUS}) and the alternative 48 MHz clock input. All these alternatives, however, are included in the schematics and are described in this document.

2.1. Distribution of Power Sources and Power Management Support

As shown in the schematics (see Section 4), a simple solution by using one jumper (JP1) may be adopted to choose between PCI V_{CC} = 3.3 V or PCI V_{AUX} = 3.3 V as the main power source for the ISP1561. The PCI V_{AUX} = 3.3 V power source was introduced in *PCI Local Bus Specification Revision 2.2*. It allows powering an add-on card and generation of the PME# signal even if the system is in a "deep power management state" and PCI V_{CC} is OFF. An

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alternative solution to using a jumper may be a simple circuit composed of a pair of MOSFET transistors that allows the detection of the presence of PCI V_{AUX} = 3.3 V and automatic selection of the input voltage.

Selection of the PCI V_{CC} = +3.3 V should be the default position of jumper JP1 in case of a standard add-on card design. The other possible position of JP1 selects PCI V_{AUX} = 3.3 V for complete Power Management tests including S3cold in case of on-motherboard or notebook. Note that pins 5 and 85 of the ISP1561 are connected to a DV_{AUX} power plane and pins 93, 108, 115 and 121 are connected to the AV_{AUX} power plane. Each of these planes is separated from V_{AUX} by its own set of inductors and decoupling capacitors.

Although most of the motherboards provide the PCI V_{AUX} power source in all system power management modes including S3cold, the PCI +5 V power supply is simultaneously interrupted with the PCI V_{CC} = +3.3 V.

Since the V_{BUS} voltage present on USB connectors is normally derived from the PCI +5 V power supply, in certain standby modes (S3cold) the devices connected to USB ports will not be powered once the +5 V power is removed. Therefore, the ISP1561 V_{AUX} is not useful in case of a standard PCI add-on card implementation for a system wake-up from S3cold. It is, however, a very useful feature for on-board and mobile application designs because it allows additional considerable power savings and also wakes-up the system by using a USB device. Obviously, the system wake-up from S3cold, generated from a USB device (USB mouse or USB keyboard) connected to the ISP1561 Host Controller must be supported in system's BIOS, hardware (a continuous +5 V must be supplied to V_{BUS}) and operating system drivers.

To be able to test the remote wake-up—especially, from those power management states in which the +5 V power source on PCI is not present (for example, S3cold)—a special connector (J1) is added on the evaluation board ver. 3.01 and above for an external +5 V source. Any external independent power supply that provides +5 V ± 5% @ 2 A stabilized can be used (for example, a standard hub power supply).

Note the distribution of the pull-up resistors in the recommended schematics. For example, to achieve correct functionality, it is recommended to connect the pull-up resistors placed on the PWEn_N and OCn_N input signals of the power switch (for example, MIC2026) to DV_{AUX}, maintaining a good condition of these signals even when +3.3 V and +5 V are OFF. The "fault flag" pins (OCn_N) of the MIC2026 are open-drain and require the presence of pull-up resistors. A 100 nF capacitor is used on each OCn_N signal to prevent false fault conditions.

CLKRUN# is implemented in the ISP1561 on pin 55. This signal is targeted mainly for mobile system designs. CLKRUN is an I/O pin. It is used by the system to safely turn-off the PCI CLK for power saving, with acknowledgement from the ISP1561 according to a predefined protocol. In the case of PCI adapter card design, CLKRUN# must be always LOW (because it is not present in the PCI connector). CLKRUN# may be directly connected to GND.

2.2. Input Clock

You can use either a 12 MHz crystal (the default recommended solution for the best EMI results) or a 48 MHz oscillator (this may be a useful alternative, typically, in the case of on-motherboard design. Both solutions for the input clock are shown in the schematics.

To use a 48 MHz clock as input, connect the clock signal to the ISP1561 pin 87 (XTAL1), pin 88 (XTAL2) can be left open and pin 1 (SEL48M) must be pulled-up as shown in the schematics.

In an add-on card configuration, normally, the 12 MHz crystal is used. In such a case, the oscillator OSC2 and R28 are not necessary. Also, pin 1 (SEL48M) must be directly connected to GND. Another possibility is using a 12 MHz clock as input. In this case, the 12 MHz-clock signal is connected directly to the ISP1561 pin 87 (XTAL1). This is similar to the case in which the 48 MHz clock is used; however, the ISP1561 pin 1 must still be connected to GND.

2.3. Selection of Number of Ports

Selection of the number of ports (2 or 4 ports) is done using the SEL2PORTS signal (ISP1561 pin 9). It must be pulled LOW (connected to GND) for normal use of all four ports. If SEL2PORTS is HIGH, only two ports (Port 1

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and Port 2) are enabled; one port from each OHCI will be used in this case for performance improvement. Details regarding the power consumption and possible power savings in a two-port configuration can be found in the ISP1561 data sheet.

2.4. Subsystem Vendor ID and Subsystem Device ID

The ISP1561 allows loading of the Subsystem Vendor ID (VID) and the Subsystem Device ID (DID) for both EHCI and OHCI from an external EEPROM. Loading of these values in the configuration registers of the ISP1561 will occur only if a value of 15H is found in byte 7 of the EEPROM. The necessary signals—I^2C-bus clock and I^2C-bus data—are defined on pins 2 (SCL) and 3 (SDA), respectively. These signals must be normally pulled-up (using a 4.7 k) to DV_{AUX}.

2.5. Legacy Support

The legacy signals (IRQ1, IRQ12, A20OUT, KBIRQ1, MUIRQ12 and SMI#) are not normally used on a PCI add-on card design. In this case, the MUIRQ12 and KBIRQ1 input signals should be connected to GND. The other signals that are mentioned in this category (that are outputs) can be left open.

Details on legacy signals and a block diagram showing correct connection of these signals in the case of on-board design can be found in the *ISP1561 Evaluation Board User's Guide (*UM10005*).*

2.6. Overcurrent Protection

The ISP1561 implements the "digital" overcurrent protection scheme.

The recommended solution for implementing an external overcurrent protection is a standard power switch with integrated overcurrent detection, such as:

- LM3526, MIC2526 (2 ports) or
- LM3544 (4 ports).

The overcurrent protection logic of the ISP1561 uses the following two pins for each USB port:

- PWEn_N: It is used to enable or disable the respective external Port Power Switch (for example, MIC2526 and LM3526).
- OCn_N: It is an input on which a fault condition on the respective USB port is signaled to the ISP1561 by the external Port Power Switching device.

The fault condition that is usually signaled by an external Power Switching Device could be an overcurrent or a thermal shutdown. The Port Power Switching integrated devices commonly implements a delay of 1 ms to 3 ms to prevent false OC_N reporting because of in-rush currents when plugging a USB device.

Once a fault condition is received, it will be detected by the operating system and the respective device driver will disable the Port Power Switch by programming the Port Power (PP) bit in the PORTSC register. This device driver is the OHCI driver in the case of an Original USB device (responsible for creating the fault condition) or the EHCI driver in the case of a Hi-Speed USB device (created the overcurrent condition). This is in accordance with the USB port allocation at the moment when the OC# signal was asserted.

A possible alternative is using a resettable fuse on each port. This has the advantage of simplicity. It, however, does not inform the operating system of the fault condition and, therefore, no message is generated to inform the user. The resettable fuse will continue to protect the port by switching "ON/OFF" as long as the overcurrent condition persists.

A possible enhancement of this scheme is connecting V_{BUS} to the OCn_N input of the ISP1561 for detection of the OC_N condition (the first time V_{BUS} is cut-off a "0" logic level will appear on the OC_N pin).

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Using only an external PMOS transistor for overcurrent protection is not possible because the ISP1561 does not implement the “analog overcurrent protection” (not measuring the current through the transistor).

3. PCB Design Recommendations

The most important checkpoints for a successful PCB design, applicable to both adapter card and motherboard design solutions, are listed as follows:

- Typically, a solution using four layers PCB (Signal1/GND/V_{CC}/Signal2) is sufficient for proper routing, allowing you to obtain good functionality and meeting all compliance tests requirements. Start your design by placing the ISP1561 chip, the major components, and routing of the high-speed DP and DM traces and clock traces. Also, a complete ‘clean’ solution for routing the power and GND (split planes) must be defined before you start routing the rest of the signals.
- The trace length for all PCI signals (except the PCI clock signal) to the PCI connector must be limited to a maximum of 1.5 inches.
- The length of the PCI clock signal from the PCI bus connector to the ISP1561 must be 2.5 ± 1 inches in length and must be routed to only one load. It must usually be ‘snaked’. Ensure that all corners of this trace are rounded. Do not use 90° sharp corners.
- Route the Hi-Speed USB differential pairs over continuous GND or power planes. Avoid crossing anti-etch areas and any breaks in the internal planes (plane splits). The minimum recommended distance to a plane split is 25 mils. You must also avoid placing a series of VIA holes near the DP and DM lines, as these will create “break areas” in the GND plane below. This is because of the clearance imposed by the manufacturing process around any VIA holes to an internal plane.
- Try to keep the length of the DP and DM traces equal. The maximum trace length mismatch between USB 2.0 signal pairs must not be greater than 70 mils.
- Maintain parallelism between USB differential signals, with the trace spacing needed to achieve 90 Ω differential impedance. To achieve the required impedance of the pair traces, it is recommended that you use 8 mils traces and keep the distance between DP and DM traces at 8 mils. These values may vary depending on the actual PCB parameters.
- Avoid corners when routing the differential pairs DP and DM. Any 90° direction change of traces must be accomplished with two 45° turns or by using an arc of an imaginary circle tangent to the DP and DM lines.
- Avoid routing the USB differential pairs near I/O connectors, signal headers, crystals, oscillators, magnetic devices and power connectors.
- Maintain the maximum possible distance between Hi-Speed USB differential pairs, high-speed or low-speed clock, and non-periodic signals. The minimum recommended distances are as follows:
  - 20 mils between the DP and DM traces and low-speed non-periodic signal traces
  - 50 mils between the DP and DM traces and clock/high-speed periodic signal traces
  - 20 mils between two pairs of the DP and DM traces.
- Avoid creating stubs for connecting the 15 kΩ pull-down resistors or for testing points. If a stub is unavoidable in the design, no stub must be greater than 80 mils.
- Route all the DP and DM lines on one layer. Do not change layers (avoid using VIAs) even to avoid crossing a plane split. It is better to place a non-split plane under Hi-Speed USB signals, ground layer or power layer. It is recommended that you place ground layer beneath the DP and DM lines.
- The maximum allowed length of the DP and DM lines for onboard solutions (or [trace + cable length] for a front-panel solution) is 18 inches.

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- A decoupling capacitor must be placed on V_{BUS} as close as possible to each USB connector. A value of about 150 µF/10 V is recommended on each port.
- The common-mode choke used (if really necessary) on the DP and DM lines must be placed as close as possible to the USB connector and must have $Z_{com} < 8\ \Omega$ @ 100 MHz and $Z_{diff} < 300\Omega$ @ 100 MHz.
- The common-mode choke, as well as the electrostatic discharge (ESD) protection components will be used only if necessary—in case the design does not pass electromagnetic interference (EMI) or the ESD tests—as these may affect the signaling quality. Nevertheless, it is recommended that you include the necessary footprints for the common-mode chokes and ESD protection components on the PCB as safeguards. The footprints must be placed as close as possible to the USB connector. Special care must be taken when placing additional components on the DP and DM lines and routing recommendations must be followed.
- Both AV_{AUX} (analog) and DV_{AUX} (digital) are derived from the V_{AUX} voltage, found on pin A14 of the PCI connector. DV_{AUX} can be directly connected to PCI V_{AUX}. AV_{AUX} is separated from V_{AUX} by an inductor and each of DV_{AUX} and AV_{AUX} uses its own decoupling capacitors.
- The design must ensure that the AV_{AUX} and DV_{AUX} power planes are isolated from the main PCI 3.3 V power plane. This is achieved by creating two separate power planes that does not come in contact with the PCI 3.3 V power plane.
- The decoupling capacitors must be placed as close as possible to the ISP1561. A good choices is the four corners of the IC as these areas will not be normally occupied by traces or other components, according to the ISP1561 pinout.
- For good EMI testing results, it is recommended that you provide a good path from the USB connector shell to the chassis ground. The USB connector shell must be connected to an isolated ground plane.

For more information, refer to the Intel® document *The USB 2.0 Platform Design Guideline, Rev. 1.0* at http://developer.intel.com/technology/usb/techlit.htm.

4. Schematics

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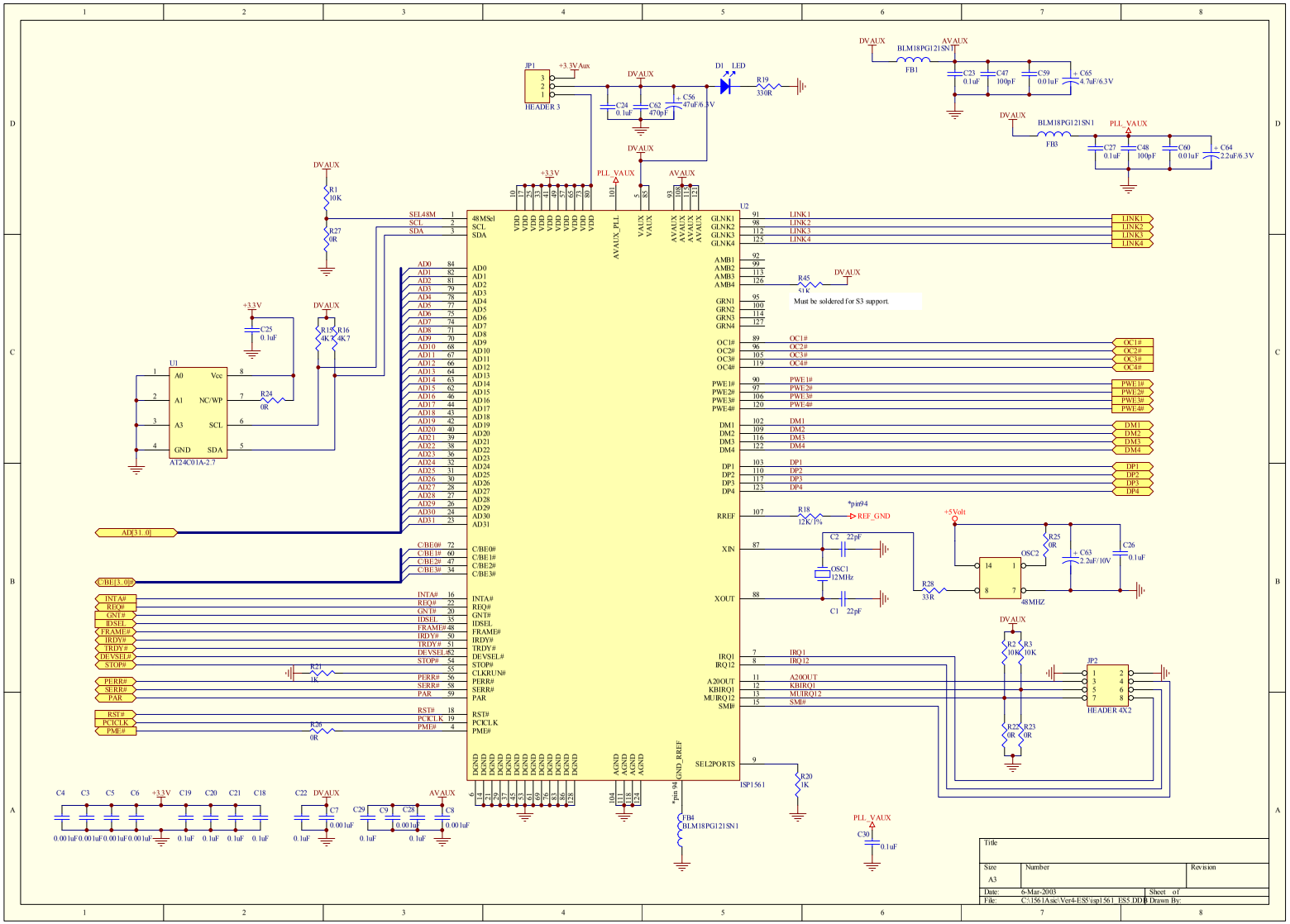
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+3.3VAux
DVAUX
D1 LED
R19
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C24
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C62
470pF
+ C56
47uF/6.3V
AVAUX
BLM18PG121SN1
FB1
C23
0.1uF
C47
100pF
C59
0.01uF
+ C65
4.7uF/6.3V
PLL_VAUX
FB3
C27
0.1uF
C48
100pF
C60
0.01uF
+ C64
2.2uF/6.3V
+3.3V
R1
10K
R27
0R
SEL48M
SCL
SDA
U1
A0
A1
A3
GND
Vcc
NC/WP
SCL
SDA
AT24C01A-2.7
C25
0.1uF
R15
4K7
R16
4K7
R24
0R
U2
48MSel
SCL
SDA
VDD
AVAUX_PLL
VAUX
AVAUX
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
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LINK2
LINK3
LINK4
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AMB2
AMB3
AMB4
GRN1
GRN2
GRN3
GRN4
R45
61K
Must be soldered for S3 support.
OC1#
OC2#
OC3#
OC4#
PWE1#
PWE2#
PWE3#
PWE4#
DM1
DM2
DM3
DM4
DP1
DP2
DP3
DP4
RREF
R18
12K/1%
*pin94
REF_GND
XIN
XOUT
C2
22pF
OSC1
12MHz
C1
22pF
+5Volt
R25
0R
OSC2
C63
2.2uF/10V
C26
0.1uF
R28
33R
48MHZ
IRQ1
IRQ12
A20OUT
KBIRQ1
MUIRQ12
SMI#
R2
10K
R3
10K
JP2
HEADER 4X2
R22
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R23
0R
SEL2PORTS
R20
1K
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C4
C3
C5
C6
C19
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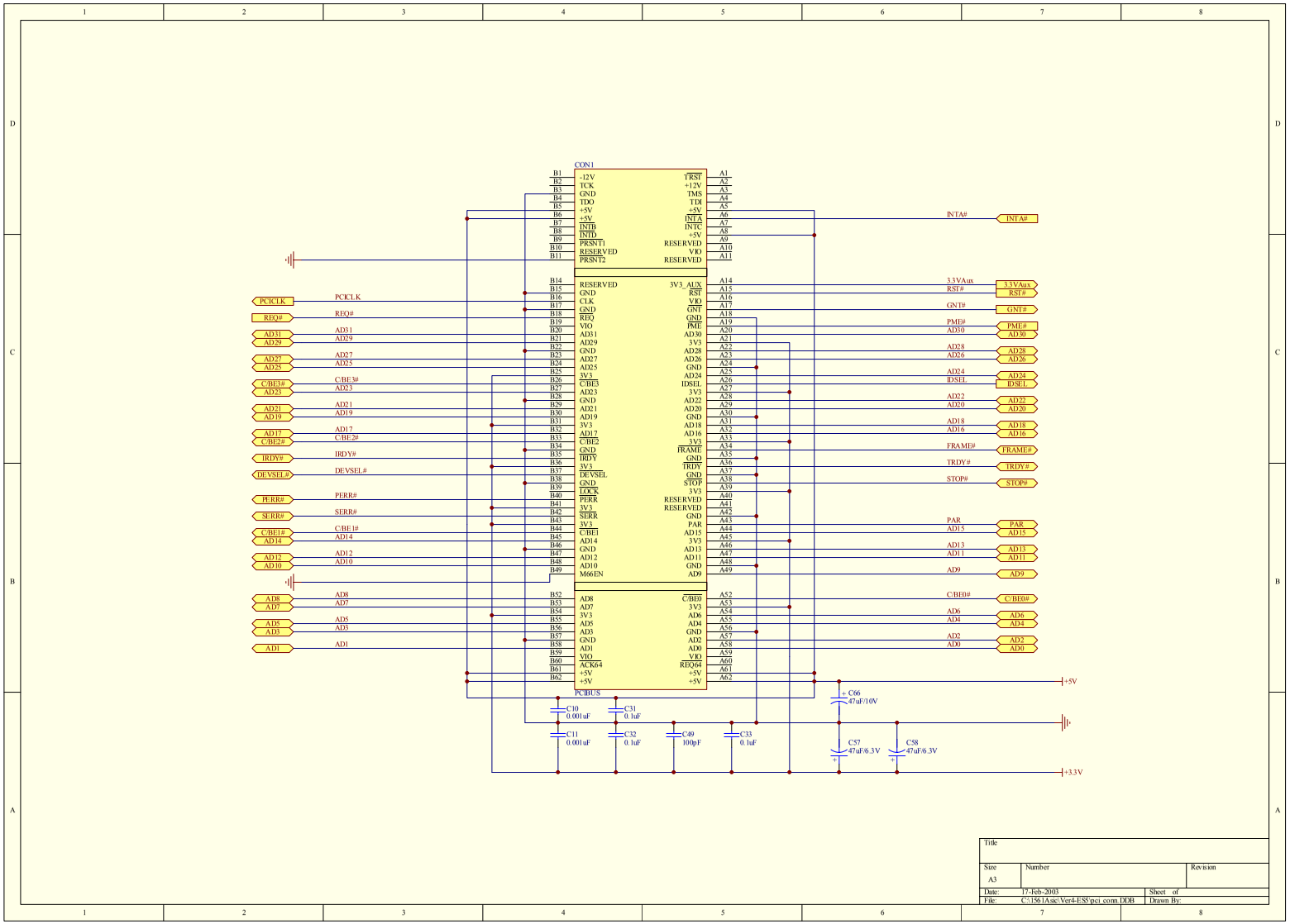

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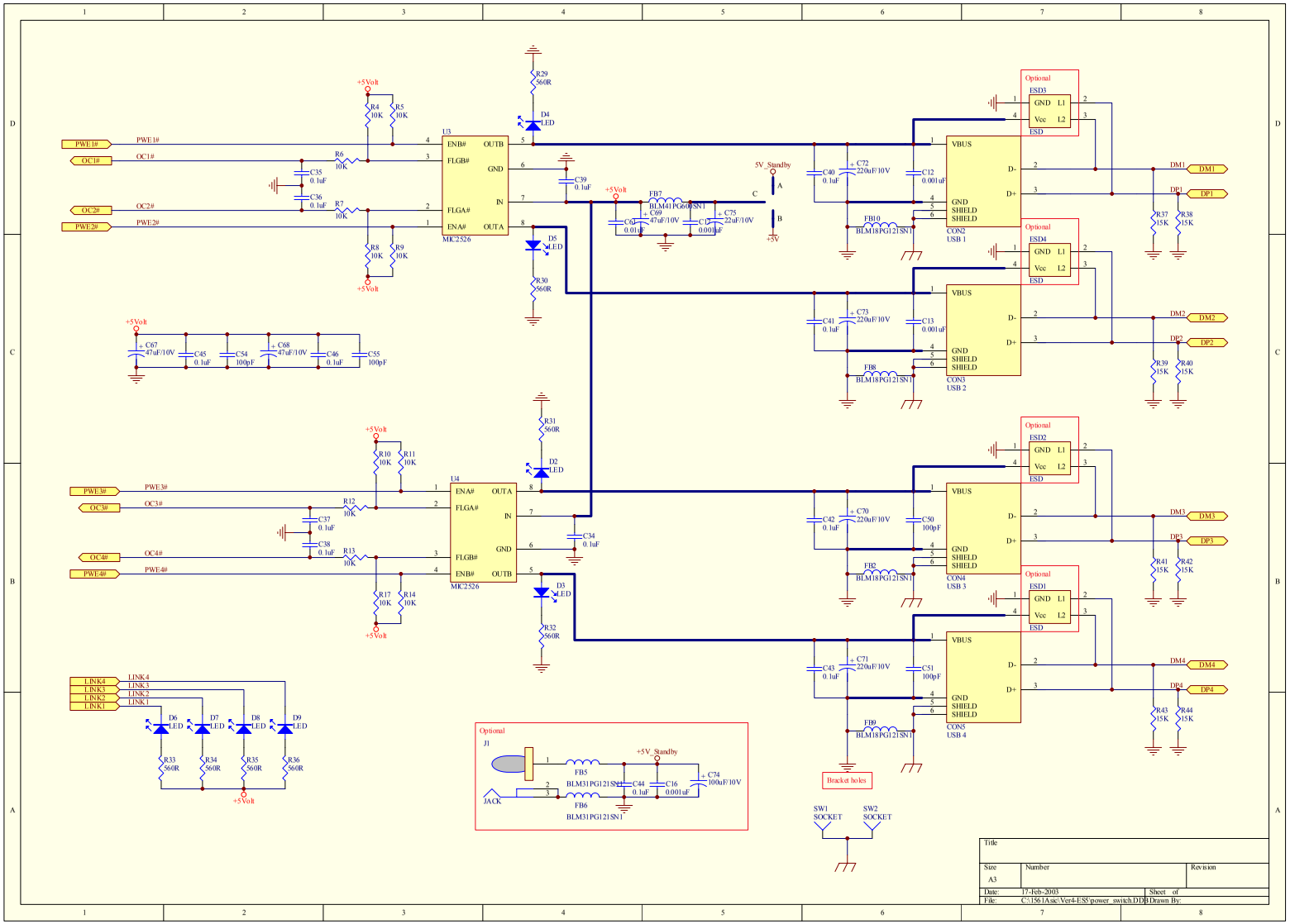
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U3
U4
VBUS
GND
SHIELD
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CON3
CON4
CON5
USB 1
USB 2
USB 3
USB 4
ESD
Optional
Bracket holes
JACK
SW1
SW2
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Drawn By:

5. References

- *ISP1561 Universal Serial Bus 2.0 PCI host controller* data sheet
- *ISP1561 Evaluation Board User's Guide*
- *Universal Serial Bus System Architecture, First and Second Editions from MindShare*
- *Universal Serial Bus Specification, Rev. 1.1 and Rev. 2.0*
- *PCI Local Bus Specification, Rev. 2.2*
- *PCI Bus Power Management Interface Specification, Rev. 1.1*
- *PCI System Architecture, Fourth Edition from MindShare.*

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